CLAIMS

1. A semiconductor structure comprising a field effect transistor (FET) having a cap-free gate and a conductive contact to a diffusion adjacent to said cap-free gate, said conductive contact being separated from said gate by only an insulating sidewall space on said gate, said insulating sidewall spacer on said gate having a height less than or equal to a height of the cap-free gate.

2. The structure as recited in claim 1, wherein said gate comprises an insulating film thin enough so a source/drain implant of the FET penetrates into said gate.

3. The structure as recited in claim 1, further comprising an implanted source/drain and wherein said implant has a dose in said diffusion, wherein said cap-free gate comprises no insulating film capable of blocking more than half said dose.

4. The structure as recited in claim 1, wherein said conductive contact extends at least partially above said cap-free gate without shorting to said gate.

5. The structure as recited in claim 1, wherein the field effect transistor is a dual work function FET.

6. A method of processing a semiconductor comprising:

a) providing a substrate;

b) forming a film on said substrate, said film having a top surface;

c) forming a hole through said film;

d) providing an insulating layer having an opening aligned to the hole and larger than the hole so a portion of said top surface of said film is exposed;

e) providing a material in said hole;

f) providing a spacer along a sidewall of said opening to shrink said opening and cover exposed portions of said top surface of said film, wherein said spacer extends to said material within the hole.

7. The method of claim 6, wherein said film is conductive, and said film is borderless to said material in said hole.

8. The method of claim 7, further comprising providing an insulating spacer along a sidewall of said hole to insulate said sidewall of said conductive film, thereby allowing said borderless contact.

9. The method of claim 6, wherein said material in said hole is conductive.

10. The method of claim 6, wherein said conductive material comprises a metal or conductive polysilicon.

11. The method of claim 6, wherein said conductive material is recessed below said top surface of said film.

12. The method of claim 6, wherein said film comprises a substantially cap-free gate conductor of a field effect transistor.

13. The method of claim 6, wherein said conductive material is a conductive contact to a diffusion.

14. The method of claim 6, wherein said providing an insulating layer comprises forming an opening in a hard mask.